Electrothermal simulation of the self-heating effects in GaN-based field-effect transistors

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We report results of the analytical and numerical investigation of self-heating effects in GaN-based high-power field-effect transistors. The problem of heat transfer in a transistor structure has been solved both analytically, using the method of images, and numerically. Two-dimensional electrothermal simulations of the GaN metal-semiconductor field-effect transistors on SiC and sapphire substrate have been performed in a framework of the drift-diffusion model. Using the physical-based simulations, we studied the dependence of the hot-spot temperature on the gate-to-gate pitch in the transistors with multiple gate fingers. Particular attention has been paid to comparison of self-heating effects in GaN transistors on SiC and sapphire substrates. The obtained results can be used for optimization of the thermal design of the GaN-based high-power field-effect transistors. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2336299]

I. INTRODUCTION

GaN-based field-effect transistors[1,2] (FETs) are considered to be excellent candidates for applications in the ultrahigh power microwave systems, power electronics, and radars operating in harsh environment.[3–6] The high breakdown voltage and large saturation velocity of the charge carriers allow these devices to handle substantial power densities. As a result, the power dissipated in GaN FETs can reach very high values and lead to substantial self-heating of the device. The self-heating and increased temperature in the transistor channel can significantly influence the current-voltage characteristics. Thus, it is important to accurately simulate thermal effects in GaN FETs, and be able to optimize the transistor structure using the physical-based simulations.

We have previously investigated the thermal effects in GaN metal-semiconductor field-effect transistors (MESFETs).[7] In this early work, we have used the simulation domain with the size comparable to the source-drain distance. Following the approach suggested by Schutz *et al.*[8] the thermal resistance of the substrate was included into the total thermal resistance and lumped with the semi-insulating (SI) GaN buffer. However, we have determined that such an approach has limitations and may lead to significant discrepancies for high power levels, multiple gate finger transistors, or several devices operating in close proximity. Specifically, the simplified approach may result in the overestimation of the hot-spot temperature.

There is substantial number of works on modeling and simulation of GaN-based transistors. Braga *et al.*[9] have simulated GaN-based heterostructure field-effect transistors (HFETs) taking into account the quantum and hot electron effects in the framework of the hydrodynamic electron-transport model. The authors have argued that hot electrons could be captured in bulk GaN by traps, which leads to a small negative differential conductivity (NDC) observed experimentally. The simulations presented in the study were limited to the relatively small source-drain biases (less than 10 V); the thermal conductivity equation was also not included into the simulations.

Nuttinck *et al.*[10] and Park *et al.*[11] experimentally studied self-heating and performed thermal simulations of AlGaN/GaN HFETs in order to estimate the hot-spot temperature. Kuball *et al.*[12] used the high spatial resolution micro-Raman spectroscopy to map the temperature distribution in the AlGaN/GaN HFETs and performed thermal simulations. In these three studies, only the thermal conductivity equation has been solved. Thus, understanding of the self-heating effects in GaN FETs is still far from being complete. There is a strong need for the reliable combined electrothermal simulating approach.

In this paper, we offer an analytical solution for the heat dissipation in GaN FET device structure together with the two-dimensional (2D) electrothermal simulations of GaN MESFETs performed using the drift-diffusion model (DDM). The simulations were performed using the software tools developed by SYNOPSYS, Inc. (formerly ISE TCAD DESSIS). The simulation approach presented for MESFETs can be readily extended to HFETs.

II. HEAT TRANSFER IN THE SUBSTRATE AND THE PROBLEM OF THE SIMULATION DOMAIN

Modern simulation tools usually have the capability of simulating self-heating in different transistors, including GaN-based FETs. At the same time, extraction of meaningful results with the help of commercial software is a challenging task. There are several limiting factors, which have to be taken into consideration while performing the simulations.[13] For example, the simulation domain usually involves only a small portion of the device structure while the heat spreads occurs over much larger area, essentially over entire substrate. To overcome this, it is normally recommended to use a large simulation domain, although no practical guidelines

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regarding the domain size are given. Here, we establish criteria for the adequate lateral dimensions of the simulation domain in order to be able to accurately simulate a high-power FET on a thick substrate using the electrothermal approach. For this purpose, let us consider the heat diffusion from the point and the linear heat sources located under the thermoinsulating coating on a substrate. The substrate, in its turn, is placed on top of a half-space heat sink. Thermal conductivity of the substrate is k_1 while the thermal conductivity of the half-space heat sink is k_2. We will solve the problem of heat transfer in such a schematic transistor structure by employing the method of images.[14,15]

The fundamental solutions of the Laplace operator in 2D and three-dimensional (3D) spaces[16] give the distribution of temperature due to the point and linear heat sources. The temperature distribution from a point heat source in 3D space is given as

$$T(\mathbf{r}) = T_0 + \frac{q}{4\pi k}\frac{1}{|\mathbf{r}-\mathbf{r}_1|}. \tag{1}$$

Here T_0 is the temperature at an infinite distance from the point heat source, which dissipates the power q, $\mathbf{r}_1$ is the radius vector of the location of the heat source. For the linear heat source, we will use notation σ instead of q to underline that these are two physical values with different dimensions: q has the dimension of power; σ has the dimension of a linear power: power per unit of length. The temperature distribution due to the linear heat source σ in the transversal plane is written as

$$T(\mathbf{r}) = T_0 - \frac{\sigma}{2\pi k}\ln\left(\frac{|\mathbf{r}-\mathbf{r}_1|}{r_0}\right). \tag{2}$$

Here r_0 is the radius of the cylindrical surface with fixed temperature T_0 around the linear heat source.

Using an analogy with a well-known electrostatic problem,[17] which can be solved by the method of images, one can consider a heat source placed in the half space with the thermal conductivity k_1 on distance d from the interface with the second half space with the thermal conductivity k_2. In this case, the distribution of temperature in the first half space, with the thermal conductivity k_1, is determined by the introduced point-heat source q and by its image αq placed in the second half space. The parameter α is determined by the expression

$$\alpha = \frac{k_1 - k_2}{k_1 + k_2}. \tag{3}$$

The distribution of temperature in the second half space, with the thermal conductivity k_2, is determined by the point heat source βq in place of considered heat source q. The parameter β is given by

$$\beta = \frac{2k_2}{k_1 + k_2}. \tag{4}$$

Note that $\alpha+\beta=1$. In the discussion to follow, we will use the ratio of the thermal conductivities $K=k_2/k_1$. The case when K equals zero corresponds to the adiabatic boundary condition on the bottom of the first half space. The case when K equals unity is for the same thermal conductivities of both half spaces. If $K\rightarrow\infty$, one has a perfect heat sink with the isothermal boundary condition on the bottom of the first half space.

Here, we employ the Rinaldi[15] approach based on the method of images to write explicitly the expressions for temperature distribution from the point and linear heat sources in the considered schematic transistor structure. The obtained expressions will be the Green functions for 3D and 2D thermal conductivity equations for given structure, thermal conductivity values, and the boundary conditions. This approach will allow us to find the distribution of the heat flow through the interface between the substrate and the half-space heat sink. Finally, it will allow us to estimate the size of the heat flow cross section in the plane of the interface between the substrate and the heat sink. Below, we refer to this cross-section size as the dimension of the substrate-bottom hot spot. This dimension also defines the size of the simulation domain required for accurate numerical modeling.

Due to the symmetry of the schematic two-layer transistor structure [see Fig. 1(a)], we can consider the doubled heat source centered in the layer with the thermal conductivity k_1 surrounded by ambient with the thermal conductivity k_2 [see Fig. 1(b)]. Following the method of images, one can write the temperature distribution in the central layer from the set of heat sources as

$$q_N = \alpha^{|N|}2q, \tag{5}$$

with the coordinates [see Fig. 1(c)] given by

$$x_N = d(1+2N), \quad N = 0, \pm 1, \pm 2 \ldots . \tag{6}$$

In the heat sink area (negative values of the coordinates), the temperature distribution is determined by a set of the heat sources expressed through

$$q_N = \beta\alpha^N 2q, \tag{7}$$

with the coordinates [see Fig. 1(d)] given by

$$x_N = d(1+2N), \quad N = 0,1,2 \ldots . \tag{8}$$

It is now possible to find the temperature distribution in the central layer for the case of the point heat source through the superposition of the temperature distribution components from all point heat sources given by Eq. (5),

$$T_1(x,r) = T_0 + \frac{2q}{4\pi k_1}\sum_{N=-\infty}^{+\infty}\frac{\alpha^{|N|}}{\sqrt{(x-d(2N+1))^2+r^2}}. \tag{9}$$

Similarly, one can find the temperature field in the heat sink half space with the thermal conductivity k_2 by superimposing temperature distributions from all point heat sources given by Eq. (7),

$$T_2(x,r) = T_0 + \frac{\beta 2q}{4\pi k_2}\sum_{N=0}^{+\infty}\frac{\alpha^{N}}{\sqrt{(x-d(2N+1))^2+r^2}}. \tag{10}$$

Now we can find the net heat-flow fraction (HFF) through the circular spot, with the radius R on the interface surface (which corresponds to the substrate bottom). It can be obtained by integration,

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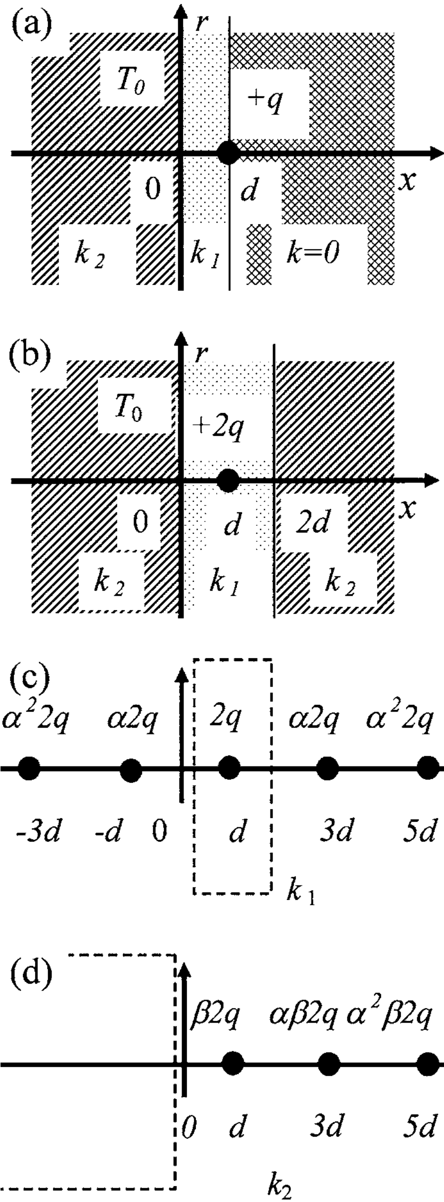

FIG. 1. (a) Schematic transistor structure used in analytical model. Here q is a heat source and d is a thickness of the substrate. (b) Equivalent symmetric structure. (c) Heat source distribution for calculation of the temperature field in the central layer (marked by dashed line). (d) Heat source distribution for calculation of the temperature field in the half-space heat sink (marked by dashed line).

$$Q(R) = \frac{1}{q}\int_0^R k_1 \left.\frac{\partial T_1(x,r)}{\partial x}\right|_{x=0} 2\pi r dr. \tag{11}$$

This integral can be expressed through the following series expansion:

$$Q = \frac{2K}{K+1}\sum_{N=0}^{+\infty}\left(\frac{1-K}{1+K}\right)^N\left\{1 - \frac{1}{\sqrt{1+\left[\frac{R}{d(2N+1)}\right]^2}}\right\}. \tag{12}$$

For the case of a linear heat source, one can write an equation for the temperature distribution in the center layer as

$$T_1(x,r) = -\frac{2\sigma}{4\pi k_1}\sum_{N=-\infty}^{+\infty}\alpha^{|N|}\ln\frac{[x-d(2N+1)]^2+r^2}{r_0^2} + \text{const}. \tag{13}$$

The temperature field in the heat sink is then given by

$$T_2(x,r) = -\frac{\beta 2\sigma}{4\pi k_2}\sum_{N=0}^{+\infty}\alpha^N\ln\frac{[x-d(2N+1)]^2+r^2}{r_0^2} + \text{const}. \tag{14}$$

One can now calculate the net heat-flow fraction Σ through the rectangular spot on the interface surface with the dimension $2R$ in the r direction and with the unit length in the z direction. It can be found by integration,

$$\Sigma(R) = \frac{1}{\sigma}\int_{-R}^R k_1 \left.\frac{\partial T_1(x,r)}{\partial x}\right|_{x=0} dr. \tag{15}$$

Finally, one derives the following expression:

$$\Sigma = \frac{1}{\pi}\frac{4K}{1+K}\sum_{N=0}^{+\infty}\left(\frac{1-K}{1+K}\right)^N \arctan\frac{R}{d(2N+1)}. \tag{16}$$

The case of the isothermal boundary condition on the substrate bottom can be easily obtained from the above expressions by letting $K\to\infty$.

Using the above expression, one can plot the dependence of the dimension R on the parameter K for different fixed values of the net heat-flow fraction. Figure 2(a) shows such dependence for the point heat source [see Eq. (12)] while Fig. 2(b) shows the dependence for the linear heat source [see Eq. (16)]. The curves on Figs. 2(a) and 2(b) are marked with the values of the net heat-flow fraction from 0.1 to 0.9. The saturated parts of the curves for the large K correspond to the case of a perfect heat sink. One can see that, even for this case, the dimension of the heat spreading area in the substrate is larger than the substrate thickness. For example, for the case of 0.9 HFF the size of the heat spreading in the substrate is 3 to 5 times larger than the substrate thickness.

The substrate-bottom hot-spot dimension increases rapidly as the thermal conductivity of the substrate becomes equal or more than the thermal conductivity of the heat sink. In the special case of $K=1$, Eqs. (12) and (16) transform into

$$Q = 1 - \frac{1}{\sqrt{1+(R/d)^2}}, \tag{17}$$

and

$$\Sigma = \frac{2}{\pi}\arctan\frac{R}{d}. \tag{18}$$

A simple calculation with $Q=0.9$ for the case of a point heat source gives $19.9d$ for the diameter of the substrate-bottom hot spot. With $\Sigma=0.9$ for the linear heat source one gets $12.6d$ for the hot-spot width. Hence, in the case of the same thermal conductivities of the two layers, the dimension of the substrate-bottom hot spot for 0.9 HFF is about 10–20 times larger than the substrate thickness. This is an interesting result, which may explain why erroneous data are sometimes obtained from computer simulation of heat flow in the device

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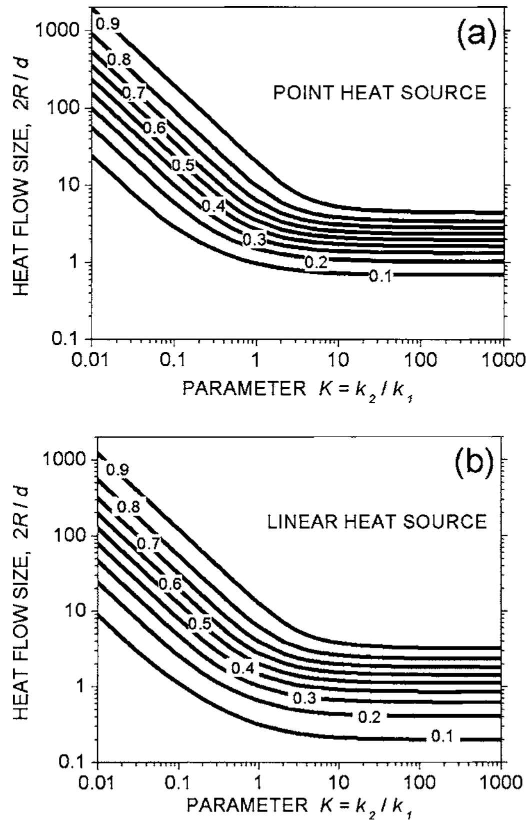

FIG. 2. Dependence of the heat spreading size in the substrate (measured in the substrate thickness units) on parameter $K=k_2/k_1$ from the point heat source (a), and from the linear heat source (b). Each curve is marked with the corresponding fraction of the net heat flow.

structure performed for not large enough simulation domains.

A typical FET has a channel with the finite width. It means that the distribution of the temperature and the heat flow in the real device structure will be somewhere between the two considered cases of the point and linear heat sources.

III. ELECTROTHERMAL NUMERICAL SIMULATION

In the previous section, we have analytically established a criterion for choosing the size of the simulation domain. In this section, we describe our approach to the simulation of GaN FET characteristics, which accurately takes into account the thermal effects. In GaN MESFETs the relatively thin doped GaN layer is deposited on SI GaN buffer of several micrometers thick over a substrate with the thickness of hundreds of micrometers. Due to the absence of inexpensive native substrates, other materials such as sapphire, Si, or SiC are usually used in GaN FET fabrication. Typically, such devices have a top passivation layer with good thermal insulation properties. Therefore, in our model, we will ignore the heat dissipation from the top surface of the device structure. Heat diffusion through the substrate bottom only will be taken into account. The validation of such a choice of the boundary condition has been given, for example, by Park *et al.*[11] We will also ignore the heat transfer along the electrodes. A detailed discussion of this approximation is offered in the next section.

We perform all simulations for the following parameters of the device, which correspond to an actual GaN MESFET described by Binari *et al.*[18] The doping concentration in the active layer is 3×10^{17} cm^{-3}; the thickness of the active layer is 200 nm; the source-drain separation 5 μm; and the gate length 1.5 μm. The *n*-type GaN active layer is deposited on the top of 3-μm-thick SI GaN buffer [a schematic of the simulated GaN-based MESFET is shown in the inset to Fig. 3(a)]. The resistivity of SI GaN buffer, reported by Binari *et al.*,[18] is rather high ($\sim$about 10^{10} Ω cm). To account for high resistivity in SI GaN buffer in our simulations we have reduced the mobility in the buffer layer accordingly. Although the transistor described by Binari *et al.*[18] has a sapphire substrate, in this paper, we consider the case of a 300 μm-thick SiC substrate. SiC has a high thermal conductivity coefficient at room temperature $k_{\mathrm{SiC}}=3.3$ W cm^{-1} K^{-1}, therefore it is a promising material for GaN transistors substrates.[19] For comparison, the thermal conductivity of sapphire at room temperature is $k_{\mathrm{sapph}}=0.35$ W cm^{-1} K^{-1} and for GaN $k_{\mathrm{GaN}}=1.6$ W cm^{-1} K^{-1}.[19] The $T^{-0.5}$ temperature dependence for thermal conductivity of GaN and T^{-1} for SiC and sapphire has been taken into account in the presented simulations.[19–21] Detailed study of the alloying, defects, and temperature on the thermal conductivity of GaN is given by Liu and Balandin.[21]

In our simulations, we consider two types of the boundary conditions for the substrate bottom. Most simulations are performed for the isothermal boundary condition of 300 K, which corresponds to the case of a perfect heat sink. The case of the external thermal resistance of 0.1 K cm^2/W lumped at the substrate bottom has been considered as the convective-type boundary. The value of 0.1 K cm^2/W approximately corresponds to the thermal resistance of the copper layer of 4 mm thickness. The adiabatic thermal boundary conditions are imposed for the side and top boundaries. The electrical conditions on the boundaries without contacts are of the reflective type, which give zero normal components of the electric field and the electron (hole) current. For the source and drain Ohmic contacts we impose the equilibrium, charge neutrality, and constant potential conditions. The boundary conditions for the Schottky gate are more complex and described elsewhere (see DESSIS manual and Ref. 22). We assume the Schottky barrier potential height of 1 eV,[23] which is consistent with the typical Pt/Au metallization for GaN. The dielectric constants of 8.9, 9.7, and 9.4 are used for GaN, SiC, and sapphire, respectively.[24–26] The effective conduction-band density of states in GaN is taken to be 2.6 $\times10^{18}$ cm^{-3}, which corresponds to the electron effective mass of $0.22m_0$ (here m_0 is a free electron mass).[23,27]

The low-field mobility dependence on the temperature and doping concentration has been described by the GaN-specific model proposed by Mnatsakanov *et al.*[28] A modified transferred-electron (MTE) model, which is able to replicate the electric field dependence of the electron drift velocity in GaN, has been used to describe the electron high-field mobility as a function of the electric field.[29] The low-field mobility for undoped GaN at temperature 300 K was assumed to be equal to 1000 cm^2/V s (433 cm^2/V s for the doping concentration equal to 3×10^{17} cm^{-3}).[27] A saturation velocity

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of 1.91×10^7 cm/s for 300 K temperature was extracted from the available Monte Carlo simulation data.[30] A linear dependence of the saturation velocity on temperature was assumed to have a negative temperature coefficient of -6.33×10^3 cm/s K. We obtained this parameter by fitting the data from the Monte Carlo simulations reported by Bhapkar and Shur.[31]

As a wide-band gap semiconductor with an energy gap of about 3.5 eV at room temperature, GaN has a breakdown electric field as high as several MV/cm, which is several times larger than that in Si and GaAs.[32] Correspondingly, devices based on GaN have larger breakdown voltages and can work at high source-drain bias. The breakdown voltages of GaN MESFET of considered design is 60–80 V as reported by Binari *et al.*[18] Chini *et al.*[33] reported the off-state breakdown of 140 V for GaN MISFET with 3 μm gate-to-drain spacing. The breakdown voltage of 900 V has been reported for FET of specific design with two field plates by Xing *et al.*[34] In our study we limit the range of the considered source-drain biases to 80 V, which is less than or comparable to the reported breakdown voltages. Experimental output characteristics of GaN-based MESFETs have been reported by a number of research groups.[1,18,35] Here we used the reported experimental data for comparison with our numerical simulations and for the model validation.

Figure 3(a) shows the current-voltage characteristics for GaN MESFET simulated for the different substrate lengths. Figure 3(b) shows the maximum temperature in the device channel as a function of the source-drain voltage. The boundary condition on the substrate bottom was assumed to be isothermal with the temperature equal to the ambient temperature of 300 K. The dash curve in Fig. 3(a) is found from the isothermal simulation. All characteristics presented in Figs. 3(a) and 3(b) are calculated for zero gate-source bias. The arrows indicate the direction of the increasing substrate length from 50 μm to 3 mm. The inset to Fig. 3(b) shows the elementary cell of the considered transistor with many gate fingers as well as the simulation domain. This picture shows that the substrate length L_{sub} (which is the lateral size of the simulation domain for the one gate transistor) coincides with the gate-to-gate pitch of the transistor with many gate fingers.

In Fig. 4, we show the results of the electrothermal simulations of the output [Fig. 4(a)] and transfer [Fig. 4(b)] characteristics for a GaN MESFET on SiC substrate. The results were obtained with the substrate length of 3 mm, which is much larger than the considered substrate thickness of 300 μm. The upper curve in Fig. 4(a) is for zero gate bias, while two others are for −2 and −4 V. The transfer characteristics were calculated for the 20 V source-drain bias.

The temperature-dependent simulation of the output characteristics of GaN MESFET on SiC substrate with the substrate length 3 mm and the external thermal resistance of 0.1 K cm^2/W lumped at the substrate bottom are shown in Fig. 5(a). The extra thermal resistance introduced to the model imitates the thermal resistance of the packaging. The ambient temperature is assumed to be 300 K. The dash-dotted curve in this figure corresponds to the case of 1 mm substrate length. For comparison, the temperature-dependent

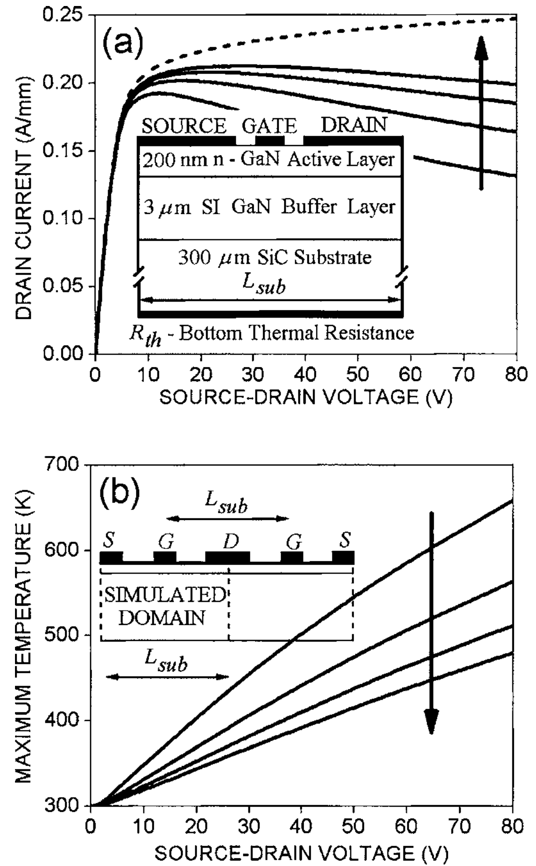

FIG. 3. Current-voltage characteristics (a) and the maximum temperature dependence on the source-drain voltage (b) obtained from the electrothermal simulations for GaN MESFET on SiC substrate. The results are shown for the substrate lengths of 50 μm, 10 μm, 200 μm, and 3 mm and the isothermal boundary condition of 300 K on the substrate bottom. The source-gate bias is zero. Dashed curve on panel (a) is for the case of the isothermal simulation. Arrows indicate the direction of the substrate-length increase. The inset to panel (a) shows a cross section of the considered MESFET. Inset to panel (b) shows the elementary cell of a transistor with multiple gate fingers and the simulation domain.

simulations of the output characteristics of GaN MESFET on a sapphire substrate with the length of 3 mm and the isothermal boundary condition ($T=300$ K) on substrate bottom are presented in Fig. 5(b). In order to compare the simulated results with experiment, in Fig. 5(c), we reproduce typical dc output characteristics for GaN-based HFETs at zero gate bias, as reported by Sun *et al.*[36] Here, the upper curve is for SiC substrate and the lower is curve for sapphire substrate. One can see in this figure a noticeable degradation of the drain current in GaN-based transistor on the sapphire substrate, which is in line with our simulations. A possible explanation of the observed stronger degradation in HFETs than in the simulated MESFETs is related to the significantly higher current density in HFETs, which results in more pronounced self-heating effects.

Figures 6(a) and 6(b) show the temperature distribution in kelvins (K) in GaN MESFET on SiC substrate with the substrate bottom lengths 50 μm [Fig. 6(a)] and 3 mm [Fig. 6(b)]. The boundary condition of $T=300$ K on substrate bottom is used in both cases. The source-drain bias was taken as 50 V while the gate bias was kept at zero. The coordinate

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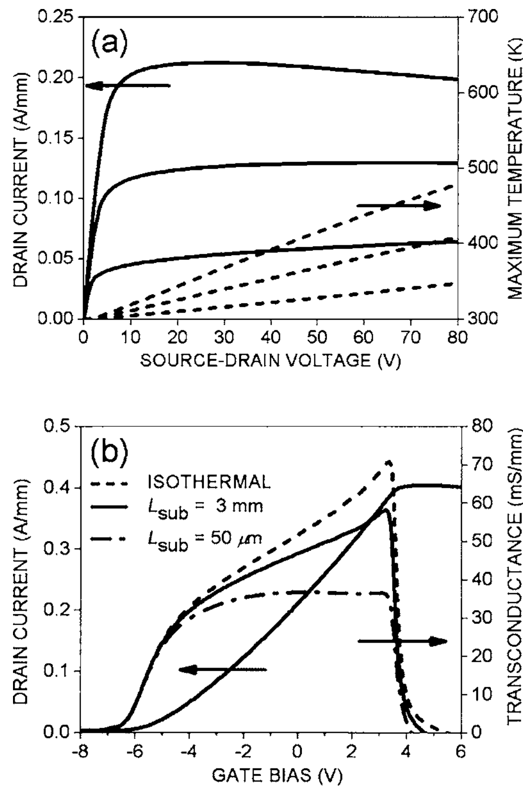

FIG. 4. (a) Current-voltage (solid) and maximum temperature-voltage (dashed) characteristics for GaN MESFET on SiC substrate for different source-gate biases. Top curve on panel (a) is for the zero source-gate bias, others for −2 and −4 V. Isothermal boundary condition (T=300 K) for the substrate bottom is assumed. (b) Transfer characteristic and transconductance (solid curves) for the source-drain bias of 20 V and for the 3 mm length of the substrate bottom. On panel (b) the dashed curve is for the case of the isothermal simulation and dash-dot curve is for the case of the electrothermal simulation with 50 μm substrate length.

x=0 corresponds to the middle of the gate. The obtained maximum temperature in the hot spot is 270 and 150 °C, respectively.

In Fig. 7, we show the dependence of the maximum temperature on length of the substrate portion covered by the simulation domain for a device on a SiC substrate with 300 μm thickness. The results are presented for the case of the isothermal (R_{th}=0.0 K cm^2/W) and convective (R_{th} =0.1 K cm^2/W) boundary conditions. The saturation of the hot-spot temperature in the case of an ideal heat sink occurs at 300 μm domain length at 150 °C while for the case of R_{th}=0.1 K cm^2/W the hot-spot temperature saturates at 190 °C (when the substrate length is larger than 3 mm).

IV. DISCUSSION AND COMPARISON WITH THE EXPERIMENTAL DATA

The output characteristics of the GaN transistors obtained from the isothermal and electrothermal simulations are in agreement with the measurements reported by Nuttinck *et al.*[10] in the pulse and continuous modes, respectively. The maximum temperature of 250 °C was reported by Nuttinck *et al.* for a transistor with many gate fingers (40 μm gate-to-gate pitch) operating at 5 W/mm. The same work reported a maximum temperature of 80 °C for a single gate device. In our simulations, 5 W/mm power corresponds to

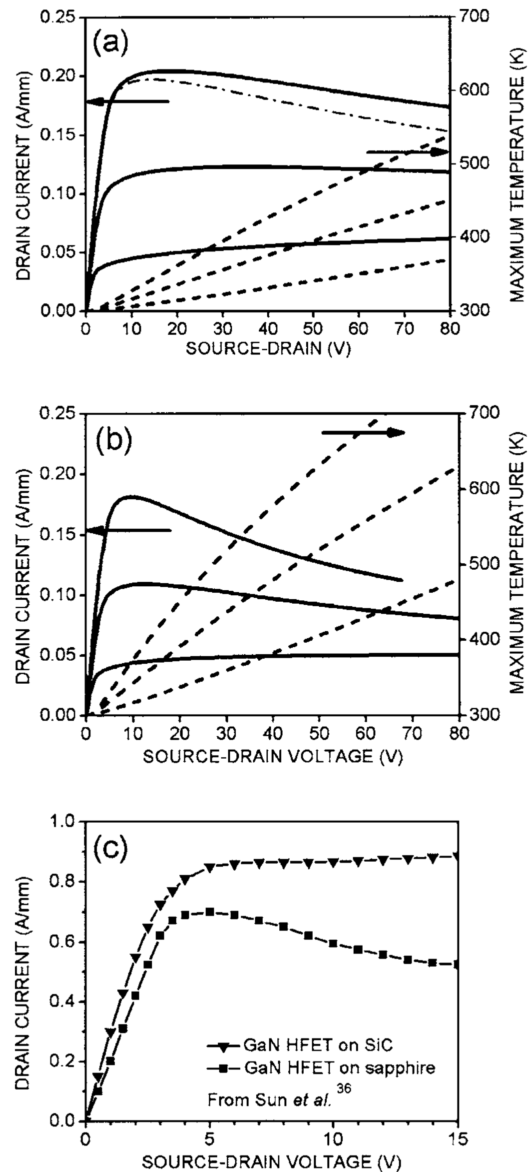

FIG. 5. (a) Current-voltage (solid) and the maximum temperature-voltage (dashed) characteristics for GaN MESFET on SiC substrate with the thermal resistance of 0.1 K cm^2/W lumped to the substrate bottom. (b) Characteristics for GaN MESFET on sapphire substrate with the isothermal boundary condition (T=300 K) on the substrate bottom. Top curves are for zero gate bias, other curves for −2 and −4 V for both (a) and (b). Temperature of the substrate bottom equals to the ambient temperature 300 K. (c) Typical dc characteristics for GaN-based HFETs on SiC (top curve) and sapphire (lower curve) substrates at zero source-gate bias reproduced from Sun *et al.* (Ref. 36).

24 V source-drain bias for L_{sub}=3 mm with T_{max}=81 °C and 28 V source-drain bias for L_{sub}=50 μm with T_{max}=171 °C [see Fig. 3(b)]. One can see that our results are in good agreement with the reported experimental data.

The total thermal resistance of the simulated single-gate finger transistor on SiC substrate is approximately 40 °C/W, which is in agreement with the value obtained by Kuball *et al.*[19] and Park *et al.*[11] We found that with the increase of the dissipated power this value can rise higher than 50 °C/W. A thermal resistance of the electrode with 150 μm length has been estimated by Wang *et al.*[37] to be 2.5×10^5 °C/W, which is much higher than the total thermal

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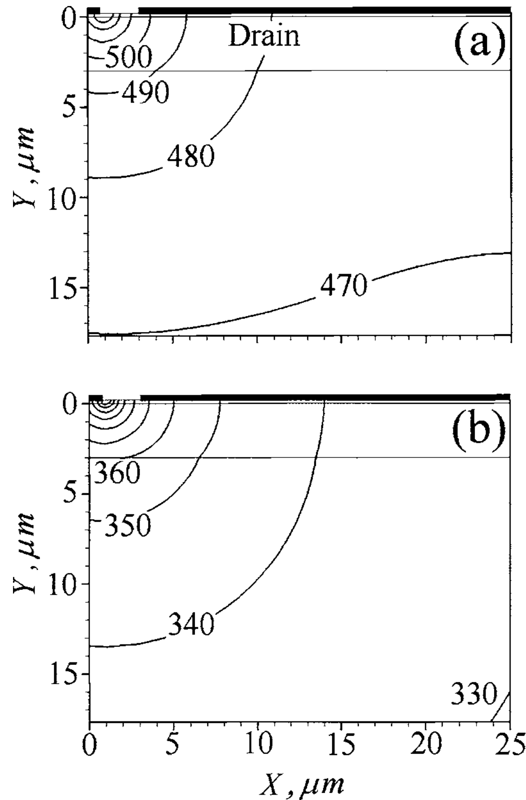

FIG. 6. Temperature distribution in kelvins (K) in GaN MESFET on SiC substrate with the substrate lengths of (a) 50 μm and (b) 3 mm. The boundary condition on substrate bottom is isothermal. The source-drain bias is 50 V and gate bias is zero. The maximum temperatures in the hot spots are 270 and 150 C, respectively. Zero x coordinate corresponds to the middle of the gate.

resistance of the considered FET. This validates our assumption that the heat transfer along the electrodes is small in comparison to heat dissipation through the substrate bottom.

The electrothermal simulations of a transistor on SiC substrate with 50 μm substrate length [see Fig. 3(a)] revealed a significant degradation of the output characteristics with the pronounced NDC region and with a relatively high temperature of the hot spot. The maximum transconductance

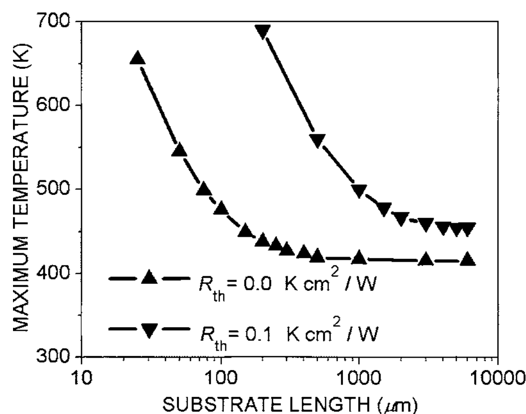

FIG. 7. Dependence of the maximum temperature on the substrate length, for the case of the convective (top curve, R_{th}=0.1 K cm^2/W) and isothermal (lower curve, R_{th}=0.0 K cm^2/W) boundary conditions on substrate bottom. Ambient temperature is 300 K. The source-drain bias is 50 V and the source-gate bias is zero.

is less than 40 mS/mm [see Fig. 4(b) dash-dot curve]. The degradation of the output characteristics in the case of 3 mm substrate length is less pronounced, and the maximum transconductance is 60 mS/mm [see Figs. 3(a), 4(a), and 4(b)]. The isothermal simulations do not lead to NDC region and result in the maximum transconductance of about 70 mS/mm [see dashed curves on Figs. 3(a) and 4(b)]. The electrothermal simulations correctly reproduce NDC region in the output characteristics, which appears due to the degradation of the electron mobility in the transistor channel with the temperature increase. In the limiting case of a very large substrate length and a perfect heat sink, the NDC effect and the hot-spot temperature decrease in value. Our numerical results pertinent to NDC are in agreement with analytical study reported by Albrecht *et al.*[38] and experimental investigations of this effect in GaN-based HFETs on SiC and sapphire substrates reported by several groups.[34,36,39–41]

Analyzing the maximum temperature dependence on substrate length presented by the lower curve in Fig. 7 (50 V source-drain bias, zero source-gate bias, and isothermal boundary condition on the substrate bottom), one can see that hot-spot temperature saturates at 150 °C when the substrate length is larger than the substrate thickness. On the other hand, if the length of the substrate is less than the substrate thickness, there is significant overheating with corresponding degradation of the output characteristics [see also Fig. 3(a)]. This result shows that the dependence of the hot-spot temperature on the substrate length, obtained from the numerical simulations, is in agreement with the analytically obtained result described in Sec. II. It also indicates that the size of the heat spreading in the substrate with the isothermal boundary condition is comparable to the substrate thickness.

Figure 5(a) and the top curve in Fig. 7 clarify how a nonideal heat sink influences the output characteristics and the hot-spot temperature. In the case of the convective boundary condition on the substrate bottom (with typical value of the package thermal resistance of 0.1 K cm^2/W) the output characteristics have more pronounced NDC region in comparison with the case of an ideal heat sink. When the boundary condition is convective, the saturated maximum temperature of the hot spot (see Fig. 7 upper curve) is 190 °C, which is 40° higher than for the case of an ideal heat sink. In Fig. 5(a), the dash-dot curve corresponds to the case of 1 mm substrate length while the solid lines correspond to 3 mm. One can see that for the 1 mm case, there is a noticeable degradation of the current-voltage characteristics in comparison with the 3 mm case. The simulation for the case of 6 mm substrate length gives practically the same result as for the 3 mm case. Our simulations show that for the thermal resistance of 0.1 K cm^2/W lumped at the substrate bottom the substrate length must be about an order of magnitude larger than the substrate thickness to obtain correct simulation results. Thus, the performed simulations confirm the conclusions obtained analytically in Sec. II. Indeed, when the heat sink is nonideal, the generated heat spreads in the substrate on distances much larger than the substrate thickness. Further analysis of the simulation results presented in Fig. 5(b), also indicate that the degradation of the output characteristics and the hot-spot temperature in MESFETs on sap-

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phire substrate is significantly larger in comparison with the case of SiC substrate. For zero gate bias and 50 V of the source-drain bias, the hot-spot temperature for transistors on sapphire substrate is 250 °C, which is 100 °C larger than that for transistors on SiC substrate.

After the simulations are performed, we can suggest that under the high source-drain bias and with not optimized thermal management, the hot-spot temperature in the active channel of GaN FET can rise beyond 600 °C. This can be somewhat higher than the safe performance temperature range estimated for GaN by Neudeck *et al.*[42] Due to the high value of the GaN breakdown field and wide band gap the device can still be far from the beginning of the avalanche or Zener breakdown. In such conditions, the thermal generation of carriers may lead to the thermal instabilities or even to the development of the irreversible thermal breakdown.[43] Since one of the proposed applications of GaN-based devices is the high-temperature electronics for the ambient temperatures beyond 300 °C,[42] the possibility of thermal breakdown in GaN FETs deserve a close attention.

V. CONCLUSIONS

We have presented the results of the analytical and numerical investigation of self-heating effect in GaN-based high-power field-effect transistors. First, the problem of heat transfer in the transistor structure has been addressed analytically, using the method of images, to determine the size of the simulation domain required for accurate numerical simulations. Second, the two-dimensional electrothermal simulations of GaN MESFETs on different substrates have been performed in the framework of the drift-diffusion model. It has been found that in the case of a perfect heat sink on the substrate bottom, the size of the heat spreading in the substrate is comparable to the substrate thickness. If the heat-sink material has the thermal conductivity approximately equal or less than the substrate, the size of the heat-spreading area on the substrate bottom is much larger than the substrate thickness. Using numerical simulations, we studied the dependence of the hot-spot temperature on the type of the substrate and on the gate-to-gate pitch in the transistors with the multiple gate fingers. The obtained results can be used for optimization of the thermal design and management of GaN-based high-power field-effect transistors.

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[1]M. A. Khan, J. N. Kuznia, A. R. Bhattarai, and D. T. Olson, Appl. Phys. Lett. **62**, 1786 (1993).
[2]M. A. Khan, A. Bhattarai, J. N. Kuznia, and D. T. Olson, Appl. Phys. Lett. **63**, 1214 (1993).
[3]Y.-F. Wu, IEEE Electron Device Lett. **25**, 117 (2004).
[4]A. Balandin, S. Cai, R. Li, K. L. Wang, V. R. Rao, and C. R. Viswanathan, IEEE Electron Device Lett. **19**, 475 (1998).
[5]S. Yoshida, H. Ishii, J. Li, D. Wang, and M. Ichikawa, Solid-State Electron. **47**, 589 (2003).
[6]S. Yoshida, J. Li, H. Takehara, and T. Wada, J. Cryst. Growth **253**, 85 (2003).
[7]V. O. Turin and A. A. Balandin, Electron. Lett. **40**, 81 (2004).
[8]A. Schutz, S. Selberherr, and H. W. Potzl, Solid-State Electron. **27**, 394 (1984).
[9]N. Braga, R. Mickevicius, R. Gaska, X. Hu, M. S. Shur, M. A. Khan, G. Simin, and J. Yang, J. Appl. Phys. **95**, 6409 (2004).
[10]S. Nuttinck, B. K. Wagner, B. Banerjee, S. Venkataraman, E. Gebara, J. Laskar, and H. M. Harris, IEEE Trans. Microwave Theory Tech. **51**, 2445 (2003).
[11]J. Park, M. W. Shin, and C. C. Lee, IEEE Trans. Electron Devices **51**, 1753 (2004).
[12]M. Kuball, J. W. Pomeroy, S. Rajasingam, A. Sarua, M. J. Uren, T. Martin, A. Lell, and V. Härle, Phys. Status Solidi A **202**, 824 (2005).
[13]V. d'Alessandro and N. Rinaldi, Solid-State Electron. **46**, 487 (2002).
[14]H. S. Carslaw and J. C. Jaeger, *Conduction of Heat in Solids* (Clarendon, Oxford, 1959).
[15]N. Rinaldi, IEEE Trans. Electron Devices **49**, 679 (2002).
[16]V. S. Vladimirov, *Equations of Mathematical Physics* (Nauka, Moscow, 1967); English translation: *Equations of Mathematical Physics* (Marcel Dekker, New York, 1971).
[17]D. V. Sivukhin, *Electricity and Magnetism* (Nauka, Moscow, 1977).
[18]S. C. Binari, W. Kruppa, H. B. Dietrich, G. Kelner, A. E. Wickenden, and J. A. Freitas, Jr., Solid-State Electron. **41**, 1549 (1997).
[19]M. Kuball, J. M. Hayes, M. J. Uren, T. Martin, J. C. H. Birbeck, R. S. Balmer, and B. T. Hughes, IEEE Electron Device Lett. **23**, 7 (2002).
[20]J. Zou, D. Kotchetkov, A. A. Balandina, D. I. Florescub, and F. H. Pollak, J. Appl. Phys. **92**, 2534 (2002); D. Kotchetkov, J. Zou, A. A. Balandina, D. I. Florescu, and F. H. Pollak, Appl. Phys. Lett. **79**, 4316 (2001).
[21]W. L. Liu and A. A. Balandin, J. Appl. Phys. **97**, 073710 (2005); Appl. Phys. Lett. **85**, 5230 (2004).
[22]W. L. Liu, V. O. Turin, A. A. Balandin, Y. L. Chen, and K. L. Wang, MRS Internet J. Nitride Semicond. Res. **9**, 7 (2004).
[23]Q. Z. Liu and S. S. Lau, Solid-State Electron. **42**, 677 (1998).
[24]M. S. Shur, Solid-State Electron. **42**, 677 (1998).
[25]M. Ruff, H. Mitlehner, and R. Helbig, IEEE Trans. Electron Devices **41**, 1040 (1994).
[26]R. C. Taber and C. A. Flory, IEEE Trans. Ultrason. Ferroelectr. Freq. Control **42**, 111 (1995).
[27]M. E. Levinshtein, S. L. Rumyantsev, and M. S. Shur, *Properties of Advanced Semiconductor Materials: GaN, AlN, InN, BN, SiC, SiGe* (Wiley, New York, 2001).
[28]T. T. Mnatsakanov, M. E. Levinshtein, L. I. Pomortseva, S. N. Yurkov, G. S. Simin, and M. A. Khan, Solid-State Electron. **47**, 111 (2003).
[29]V. O. Turin, Solid-State Electron. **49**, 1678 (2005).
[30]M. Farahmand, C. Garetto, E. Bellotti, K. F. Brennan, M. Goano, E. Ghillino, G. Ghione, J. D. Albrecht, and P. P. Ruden, IEEE Trans. Electron Devices **48**, 535 (2001).
[31]U. V. Bhapkar and M. S. Shur, J. Appl. Phys. **82**, 1649 (1997).
[32]M. Trivedi and K. Shenai, J. Appl. Phys. **85**, 6889 (1999).
[33]A. Chini, J. Wittich, S. Heikman, S. Keller, S. P. DenBaars, and U. K. Mishra, IEEE Electron Device Lett. **25**, 55 (2004).
[34]H. Xing, Y. Dora, A. Chini, S. Heikman, S. Keller, and U. K. Mishra, IEEE Electron Device Lett. **25**, 161 (2004).
[35]C. Gaquiere, S. Trassaert, B. Boudart, and Y. Crosnier, IEEE Microw. Guid. Wave Lett. **10**, 19 (2000).
[36]J. Sun *et al.*, IEEE Electron Device Lett. **24**, 375 (2003).
[37]L. Wang, T. A. Fjeldly, B. Iniguez, H. C. Slade, and M. Shur, IEEE Trans. Electron Devices **47**, 387 (2000).
[38]J. D. Albrecht, P. P. Ruden, S. C. Binari, and M. G. Ancona, IEEE Trans. Electron Devices **47**, 2031 (2000).
[39]R. Gaska, Q. Chen, J. Yang, A. Osinsky, M. A. Khan, and M. S. Shur, IEEE Electron Device Lett. **18**, 492 (1997).
[40]R. Gaska, A. Osinsky, J. W. Yang, and M. S. Shur, IEEE Electron Device Lett. **19**, 89 (1998).
[41]J. Kuzmik, P. Javorka, A. Alam, M. Marso, M. Heuken, and P. Kordos, IEEE Trans. Electron Devices **49**, 1496 (2002).
[42]P. G. Neudeck, R. S. Okojie, and L.-Y. Chen, Proc. IEEE **90**, 1065 (2002).
[43]V. O. Turin and A. A. Balandin, Mater. Res. Soc. Symp. Proc. **892**, FF13–06 (2006).

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